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INFLUENCE OF U.S. CRYPTOLOGIC ORGANIZATIONS ON THE DIGITAL COMPUTER INDUSTRY

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ERRATA: "Influence of U.S. Cryptologic Organizations On The Digital Computer Industry" by Samuel S. Snyder (Published May 1977 by National Security Agency, Fort George G. Meade, Maryland)

Page	Line	Correction
1	12	After "on Computers" insert: (17)*
1	12	After "magazine COMPUTER" insert (18)
1	14	After "of the time." insert: (14), (15), (16)
1	--	After bottom line, add: * See References, p. 35-36
2	--	(bottom of page), Delete footnote; delete asterisk on line 7.
5	16	After "security." insert (13)
5	28	"J. W. Coombs" should be "J. M. Coombs"
6	7	Delete "3,500 rpm." and substitute: "240 rpm, equivalent data transmission rate 20,000 pulses/sec."
8	6	After "Research. (10)" insert: "E.R.A. also published a book (11) summarizing the status of electronic digital computing technology as of 1950, one of the earliest publications of its kind."
22	20	Before "As already" insert: "In 1962 IBM designers who participated in STRETCH collaborated in publication of a book, edited by Werner Buchholz (12) which details the STRETCH design experience; Chapter 17, "A Non-Arithmetic Extension," describes NSA's HARVEST."

S.S.SNYDER, [redacted]
December 1977

ACKNOWLEDGEMENTS

Because many of the developments mentioned in this account of NSA's computer industry impact occurred many years ago, it was essential that the author consult numerous official records and reports, to supplement his own recollections based on first-hand experience. To those officials who made possible access to such documents, the author expresses sincere thanks for their support.

The author also is pleased to acknowledge the assistance of many technical people -- employees, former employees, and affiliated non-employees of NSA -- who gave of their time and technical expertise to read drafts, catch errors, or volunteer suggested improvements. Because there was much overlapping of interest areas, it would be impossible to connect individual subjects to specific personal contributions.

The author finally assumes sole responsibility for the use made of and conclusions drawn from his source materials.

SAMUEL S. SNYDER

May 1977

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INTRODUCTION. During the 1970's there has been a great increase in publication of articles and books on the historical aspects of the computing field. In 1971 and 1972 the Association for Computing Machinery (ACM) sponsored observances of the 25th anniversary of its founding. Special honors and awards have been heaped on many of the founding fathers and mothers, both personally and posthumously. Last fall the COMPCON-76 was held in Washington, D.C. in connection with the IEEE Computer Society's 25th anniversary celebration. Part of that conference featured a "pioneers' gathering" which was attended by many notables in the field. In December 1976, as part of the Computer Society's anniversary observance, the Society published special issues of the IEEE Transactions on Computers and of the Society's magazine COMPUTER. These journals and others contain reminiscences and chronologies of particular interest to those of us who shared the experiences of the time. More important, such writings can contribute to the education of the younger generations of computer specialists, who usually show a keen interest in learning about "the olden days."

An unfortunate aspect of all such historical accounts of computer lore is the omission (conspicuously, to some of us) of mention of the National Security Agency (NSA), or of the contributions by that Agency which helped in laying the foundation of the computer industry. The NSA over the years has been required to observe a policy of anonymity, and with good reason. But, in this age of maturing appreciation of the role of computers in nearly all civilized endeavors, it is time for acknowledging that NSA, too, uses computers. In fact, that Agency's contributions to the computer industry have been outstanding. This article relates for the first time some of the details behind the NSA computer story: Appendix A, "Chronology of NSA Computer 'Firsts'," encapsulates several highlights.

The reader will notice the conspicuous absence of remarks upon software efforts at NSA. While this side of the Agency's operations received its proper share of support, discussion of software systems has been omitted because of the key word "influence" in our title. In other words, whereas NSA instigated significant innovative software advances, an exceptional influence on industry software systems isn't easily demonstrated.

NON-NSA BEGINNINGS

The U.S. computer industry is one that might not have gotten off the ground at all without the stimulus and financial support of the U.S. government. The details of the Army Ordnance wartime requirement for assistance in calculation of ballistic tables and the creation of a team of engineers and mathematicians at the University of Pennsylvania's Moore School of Electrical Engineering to design and build ENIAC are well known. (1) (2)* Also, the design and construction of UNIVAC for the Bureau of the Census, and of RAYDAC by the Raytheon Corporation for Naval Research Labs. are important pioneering stages in early computer history. In these, the Bureau of Standards exerted important influences as supervisor of the contracts and in technical guidance. Table 1, showing the important first-generation computers supported partly or wholly by U.S. funds, conveys some idea of the importance of government support in the early days of the computer:

Table 1. FIRST-GENERATION DIGITAL COMPUTERS SUPPORTED WHOLLY OR IN PART BY U.S. GOVERNMENT FUNDING

EDVAC	Moore School of Electrical Engineering, University of Pennsylvania
I.A.S.	Institute for Advanced Study, Princeton, N.J.
RAYDAC (Orig. "HURRICANE")	Raytheon Corporation, Waltham, Mass.
SEAC	National Bureau of Standards, Washington, D.C.
SWAC (Orig. "ZEPHYR")	National Bureau of Standards, Institute for Numerical Analysis, UCLA
UNIVAC	Electronic Control Company (later: Eckert-Mauchly Computer Corp., Sperry-Rand Corp.)
WHIRLWIND	Massachusetts Institute of Technology Servo-Mechanisms Laboratory, Cambridge, Mass.

* See References, p. 35-36

MOORE SCHOOL LECTURES; I.A.S. REPORTS. By the time ENIAC was completed, in February 1946, John W. Mauchly and J. Presper Eckert, its designers, had fairly clear ideas about the kinds of features a modern general-purpose computer should have. For example, besides high-speed storage for both instructions and data, the computer of the future should have some kind of "discriminate" instructions which would make possible the modification of the course of problem solution. The experience in building and operating ENIAC certainly helped, particularly in emphasizing certain features a computer should not have. The total storage capacity of ENIAC was only 20 numbers, and the method of setting up problems to be solved consisted of plugging up, in proper sequence, large cables interconnecting the registers containing numbers to be operated upon. Also, while ENIAC's circuits were quite fast enough, it contained 18,000 electron tubes, a prohibitively large number.

Besides the people at Moore School, several other research centers and universities had begun making plans for design of large-scale computers. The completion of construction of ENIAC provided the trigger for the proposal for a conference, or series of lectures, in which outstanding researchers could report on their work. The Moore School was a natural setting, and the Office of Naval Research, U.S. Navy, and the Ordnance Department, U.S. Army, provided joint sponsorship. The lectures were given 8 July--31 August 1946 and the invited participants included representatives from 20 organizations, governmental and private. The names of speakers and titles of the talks in the complete program, "Theory and Techniques for Design of Electronic Digital Computers," are reproduced in Appendix B.

The Moore School lectures were noteworthy in several ways. Logical design for both single-address and multi-address instruction systems were described. Engineering principles were presented for dealing with arithmetic operations, as well as several systems for constructing practical computer memories. Numerical methods for attacking mathematical problems were proposed, suitable for use in digital computers. Among the lecturers' names, that of Dr. John von Neumann is worth noting, since he contributed, as a Moore School consultant, a 1945 report (3) in which many of the logical design suggestions were presented for the first time. Also, in June 1946, the first of two important Institute for Advanced Study reports (4) (5) appeared. These reports contained detailed discussions of von Neumann's ideas for computer organization and construction, and basic principles, with examples, showing how to program and code problems. The proposed computer logic, which came to be known as "the von Neumann machine," has proved to be the basic system followed in most computers until recent times. Thus, the Moore School lectures and the I.A.S. reports can be said to have laid the foundation for the modern computer industry.

PRE-COMPUTER NSA

Before formation of the Defense Deparment, the NSA's principal predecessors were Navy's Communications Supplementary Activities, Washington (CSAW) and Army Security Agency (ASA). Both CSAW and ASA performed for their respective departments important cryptologic functions.

Such activities always were able to command good support and security protection, but particularly this came to a peak during World War II. From about 1935, CSAW and ASA both began to make good use of machines in support of their mission; an integral and continuing feature was their punched-card installations. Before the advent of modern digital computers, their punched-card machines constituted the backbone of machine support; in fact, in general purpose applicability, the punched-card installation was the natural predecessor of the modern computer. In addition, both agencies built or had built under contract several special-purpose machines. CSAW, particularly, enlisted the support of several contractors to design and build special-purpose equipment; in some cases these were specialized as to problem and thus were of no use on any other job. In several other instances, the specialization constituted a specific function, such as comparing or counting; these machines had limited applicability, but were not confined to a single problem. It is worth pointing out that machines built in this "pre-computer" era utilized high-speed digital circuits similar to, and definitely antedating techniques later used in electronic digital computer technology. During World War II Navy used Eastman Kodak, National Cash Register, and several other firms to plan and build these machines. M.I.T.'s Vannevar Bush provided some of the ideas for these early equipments. The ASA utilized the services of Bell Telephone Laboratories during the war to design and construct a large complex of relay equipment which was dedicated to one particular problem. The ASA and CSAW punched-card equipment installations grew phenomenally; of particular interest was a series of special-purpose attachments built for the most part by IBM for operation with the IBM Tabulators. These in effect multiplied many-fold the power of the standard punched-card complex. Much of the effort by IBM which resulted in special-attachment design and construction was part of that company's support for the war effort. An arrangement for such work to be done at cost, together with availability of cleared company personnel, facilitated speedy action in emergencies. ASA's and CSAW's close collaboration with companies who assisted them in pre-war and World War II assignments provided valuable experience for these companies in producing solutions to data processing jobs similar in technique to those which these firms were to face in later computers-for-business assignments.

In most of the foregoing machine design jobs done by outside contractor, it was necessary to bring contractor personnel into a classified problem area; that is, security clearance for selected personnel was required. This requirement, and the necessity to observe physical security regulations, plus the feeling on the part of contractors that such limited-application efforts for government were not profitable, resulted in refusals by several firms to accept such machine-design contracts after WW-II. Thus it was that, at the end of the war, a group of Naval officers who were acquainted with this situation and particularly were technically able to provide continuing guidance for such machine support in the future, banded together and formed Engineering Research Associates, Inc., (E.R.A.). Navy's Bureau of Ships provided a blanket contract and arrangements for clearance and security. E.R.A. thus began in 1946 what became a most successful arrangement for designing equipments for use by CSAW. The company's operations were regulated by a BuShips contract under which a number of "tasks" could be assigned with minimum notice as long as funds were available. One significant aspect of the Navy's procedure for supervising work under this contract was the BuShips' system for inspection and quality control. Undoubtedly it was largely because of strict adherence to this policy that E.R.A. was able to maintain an excellent record of delivering equipment that "worked." Most of the machines built under this contractual arrangement were quite specialized as to function. Their engineering technology was similar to that being developed for electronic general-purpose digital computers.

J. W. Coombs (6) in a report at the 1947 National Electronics Conference, described work on one of the early tasks, assigned to E.R.A. in August 1946 to investigate magnetic recording on drums and disks, among other things. One of the first models constructed to test magnetic drum recording used an aluminum drum whose magnetized surface consisted of paper magnetic tapes glued to the drum's surface. Information was recorded statically, advancing the drum about 8 steps per second, by use of a ratchet which moved on signals from the input punched paper tape reader. Thus holes in the tape were recorded as magnetic marks on the drum. After recording, the drum was rotated at 225 rpm and signals could be read, erased and rewritten on the same track at a rate of 20,000 pulses per second.

Two new tasks were assigned, calling for construction of practical special-purpose machines using magnetic drums to store data for analysis. Task 9, GOLDBERG, was assigned in 1947; it was to be a comparator-like system with statistical capabilities. Early in 1948 work on Task 21, DEMON, was authorized. DEMON was to use data stored on the drum to perform a specialized version of table look-up. Both used large 34-inch-diameter drums which rotated at 3,500 rpm. Although GOLDBERG was assigned earlier, the DEMON project was completed first, and the first of five DEMON equipments was delivered in October 1948. The magnetic drum memory on DEMON was, as far as we know, the first drum memory in practical operational use in the United States. When the first DEMON was delivered, operation of electronic equipment containing large numbers of electron tubes was still in infancy. Besides routine provisions for cooling, it was found that many tubes burned out at initial power-on. A procedure for identifying "marginal" components was tried and found to be successful: each day, voltages were systematically lowered on separate racks of equipment. Marginal checking on DEMON is believed to be the first regular use of this technique in routine equipment maintenance.

E.R.A. built several other machines for NSA and other sponsors which used magnetic drums for storage. Later improved models utilized sprayed magnetic coating instead of tapes, and were also more compact. The last built for NSA were those delivered with the ATLAS computers, described below. Another example worthy of note is the ABEL computer. ABEL was built by CSAW engineers in about four months in 1949, a slow-speed relay analog of ATLAS I. Its drum memory, built by E.R.A., was identical to those used on one of the special-purpose machines. ABEL was used primarily for training ATLAS programmers, but also computed many tables of reference material. After being in successful operation for almost two years, ABEL was donated to the Office of Naval Research for use in support of the Logistics Research Project, on the campus of the George Washington University. The machine, renamed "ONR Relay Computer," is described in a 1952 report [7] by J. Jay Wolf.

NSA FIRST-GENERATION COMPUTERS

ATLAS I, ATLAS II. Among those attending the lectures at Moore School was LCDR James T. Pendergrass, representing Navy's CSAW. His supervisor had participated in consultations with Dr. von Neumann and others regarding the new computer designs being proposed, and picked LCDR Pendergrass to attend the lectures and learn of computers' possible applicability to their problems. Pendergrass was particularly impressed by the versatility promised by the proposed designs, since up to that time most machines were built to attack a particular problem. This special-purpose approach often had proved to be expensive and time-consuming. In some situations, also, the effort turned out to be a complete waste when a problem disappeared by the time a special machine had been designed and constructed. The prospect of having equipment capable of working on any of a whole range of problems was exciting, and LCDR Pendergrass' report conveyed that possibility convincingly, by including actual sample programs. Within a few months, negotiations between CSAW and E.R.A. resulted in establishment of Task 13, providing for design and construction of the ATLAS computer (from ATLAS, the mental giant, in comic strip BARNABY). Approximately one year later (November 1948) E.R.A. submitted a report to the National Bureau of Standards containing the description of a computer with design similar to that of ATLAS. [8] [9].

ATLAS' logical design was patterned after that of the Institute for Advanced Study (IAS) machine; M.I.T.'s WHIRLWIND, another machine based on the von Neumann principles, was already under construction about this time. The M.I.T. reports on WHIRLWIND were made available to ATLAS planners, and provided valuable support during early stages of ATLAS design. ATLAS differed in word size from the IAS and WHIRLWIND machines, but the instructions for all three were of the one-address type, which turned out to be characteristic of most early parallel machines. The original proposal for the ATLAS computer called for internal high-speed memory using the Selectron, a specially-designed electrostatic tube being developed at RCA's Princeton Laboratories for the IAS computer. Unfortunately, however, at the time Task 13 was assigned, the Selectron had not attained the reliability required for computer use, so the decision was made to substitute a magnetic drum type of memory. (It may be of interest to note that the only operational set of Selectron tubes was that used in RAND Corporation's JOHNNIAC, an IAS-type computer finished March 1954.) The drum memory for ATLAS was much improved over the DEMON drums, and its access time (time required to locate and read a word from memory into the arithmetic unit, or vice-versa) was considerably shorter than that of the earlier drums (17 milliseconds instead of approximately 250 maximum per drum revolution). The drum memory for ATLAS is believed to be the first in which drum locations ("addresses") were permanently recorded electronically. E.R.A. in December 1947 described their drum researches in a report to the Office of Naval Research. (10) ATLAS' capacity was 16,384 words of 24 bits (binary digits); the feature of "interlace plugging," added after it was delivered, aided the programmers in improving the access time by orders of magnitude. Actual best access time thus was reduced to 32 microseconds in cases where the operand or instruction could be located optimally. Table 2 lists the ATLAS instructions. ATLAS was delivered in December 1950, and a second machine of identical design was delivered March 1953.

Several months before ATLAS was delivered, a proposal was under way for design of a successor, to be called ATLAS II. Its logic design was unique, believed to be the first computer with two-address instructions. Its high-speed memory was built with electrostatic tubes (so-called "Williams tubes"); there was also a medium-speed drum memory similar to the one used in ATLAS I. ATLAS II was delivered in October 1953, and a second ATLAS II using magnetic cores for high-speed memory instead of electrostatic tubes, was delivered in November 1954. Incidentally, the second ATLAS II is believed to be the first core memory computer delivered to a customer in the United States. All four machines (two ATLAS I's and two ATLAS II's) gave excellent service for six to eight years.

E.R.A. planned to market the ATLAS I commercially, with the designation "ERA 1101," which was the binary equivalent of the ATLAS I task number (13). However, only one such machine was built (for E.R.A.'s Arlington office), because the commercial version of ATLAS II (UNIVAC Scientific 1103), already under way, was a more powerful computer.

TABLE 2

ATLAS INSTRUCTION CODE

Clear Add

Hold Add

Clear Subtract

Hold Subtract

Vector Add

Fill Q

Substitute Digits

Absolute Clear Add

Absolute Hold Add

Absolute Clear Subtract

Absolute Hold Subtract

Shift A Left

Shift Q Left

Substitute Execution Address

Split Clear Add

Split Hold Add

Split Clear Subtract

Split Hold Subtract

Store A

Store Q

Clear Add Plus One

Clear AR

Clear Add from Q

Hold Add from Q.

Transmit A to Q

Q Jump

Jump

Sign-Conditional Jump

Zero-Conditional Jump

Clear Logical Multiply

Hold Logical Multiply

Print Only

Print and Punch

Intermediate Stop

Optional Stop

Final Stop

Clear Multiply

Hold Multiply

Divide

Optional Jump

Pass

ABNER. Not long after receiving a copy of Pendergrass' October 1946 report on the Moore School lectures, ASA analysts began studies of all extant computer proposals. The machines considered (only paper proposals of course; none were built) were Raytheon's RAYDAC, UNIVAC, and EDVAC in addition to ATLAS. ASA analysts wrote experimental programs, estimated operation times to execute typical problems, and visited computer planners at each location. The conclusion of the ASA group after these studies was a recommendation to procure a four-address computer like EDVAC. The National Bureau of Standards assisted ASA analysts and engineers, and when the decision was made for ASA to build its own machine, NBS also made arrangements for subcontracts for mercury delay memory and for magnetic tape drives, from Technitrol Corporation and Raytheon respectively. Design and construction of a machine (named "ABNER") was just getting under way, when ASA analysts began consideration of plans for a future improved computer. It was apparent that the elementary computer instructions being programmed to execute typical cryptologic jobs were resulting in excessive operation times and such jobs were clumsy to implement. To lessen the programmers' burden, a series of special-purpose instructions was worked out, with the help of ASA engineers. By the time this additional set of instructions was perfected, the first machine was already partly built, but it was found that the new features could be incorporated in the first machine without excessive delay or additional hardware. So it was decided to add the new analytic instructions to ABNER. Instead of a total instruction set of 15 orders, the new code of orders totaled 31, using a five-bit operation symbol. This ABNER instruction set was unique, undoubtedly the first which placed primary emphasis upon non-arithmetic operations. The complete set of orders is listed in Table 3.

NSA support for commercial computer developers is exemplified in the case of ABNER in the contract for mercury delay line memories, with Technitrol Corporation, and in NSA's purchase of several magnetic tape drives from the Raytheon Corporation. A second model of ABNER also gave Technitrol an opportunity to further its computer expertise; the second machine was entirely built by Technitrol. It was a logic copy of the first ABNER; however, it was much improved in construction detail, and included additional high-speed memory. The two models of ABNER became operational in April 1952 and June 1955.

TABLE 3

ABNER INSTRUCTION CODE

Stop

Provisional Stop

Halt

Auxiliary Order

Tape (Block)

Tape (Word)

Print Upper

Print Lower

Comparison

Comparison Count

Full Multiplication

Expand Transfer

Random Jump

Skip

Full Division

Subtraction

Swish

Selective Replacement

Pattern Count

Shift and Replace

Pentabit Transfer

Equality

Equality Count

Low Order Multiplication

Mod Within Words

Short Multiplication

Pentabit Mod

Division

Cyclic Transfer

Addition

Decabit Mod

A few additional words about the ABNER instructions are believed justified. A "repetition" feature, not listed as an instruction in Table 3, was available for use in connection with many instructions. By using "0000" (normally not a possible address) in designating next instruction address, that instruction would be automatically executed again and again, with automatic operand address modification before each repeated execution, until "halted" by a Halt-number coincidence, set up by the "Halt" instruction just preceding. Furthermore, an "accumulate" feature could be activated as an option in conjunction with repetition while using one of several arithmetic instructions, so that, for example, the summation of a series of numbers could be performed with a single instruction setup. Note that the automatic address modification which was part of the repetition feature is similar to the "indexing" which later was a design feature in many commercial computers. The repetition feature, a "first" for ABNER, later made its appearance in the instruction codes of ATLAS II and several commercial computers. Other instructions particularly useful in cryptologic and other data processing applications were the several "modular" and "count" instructions. And undoubtedly most powerful of all was the "Swish" instruction, which simulated the action of a high-speed comparator. As far as is known, no other computer included among its instructions any one instruction approaching the Swish in sophistication. The HARVEST System, described in a subsequent section below, included a Streaming Unit which was based upon the same principles, and which surpassed ABNER's Swish in both speed and complexity.

NOMAD. Not all of the research and development efforts were successful. Actually, NSA's development projects yielded useful equipment in a surprisingly large proportion of cases. When one considers that most of the projects under discussion had not been tested or perfected for quantity production, the record is indeed quite good. The following story of NOMAD, an unsuccessful development, is included for three reasons:

(1) The original impulse to plan such equipment was on the right track -- in fact, quite advanced for its time. A later successful development proved this.

(2) The experience gained in the course of the project was valuable both for technical and management personnel involved.

(3) The contractor later utilized NOMAD logic ideas, circuits, and magnetic tape developments in marketing a commercial computer system.

As early as January 1950, when the Agency's first two computer projects were under construction, but none was in operation anywhere in the United States, a proposal was made for a large-scale super-speed sorting machine. The proposed machine was called "NOMAD" (a wanderer), based on the idea that data being sorted, that is, rearranged on magnetic tapes, have no fixed address. E.R.A., under Task 3 of the BuShips contract, had made feasibility studies which produced tentative design specifications of a proposed computer. In 1951 the decision was made to push such a project by soliciting competitive bids to respond to a Purchase Description. In September 1951 the Raytheon Corporation was selected and awarded a letter contract, and in May 1952 a definitive contract was signed, on a cost-plus-fixed-fee basis, for design and construction of the NOMAD system.

One of the most critical components of NOMAD was the rather massive magnetic tape system, which was called Primary Internal Tape Storage (PITS). The tapes were three inches wide, contained 36 information channels, and the tape transports were planned to move at 120 inches per second. In order to achieve maximum information stored on a reel and still have an inter-record gap between blocks for starting and stopping tape reels, information was packed solid, one block after another. It was designed

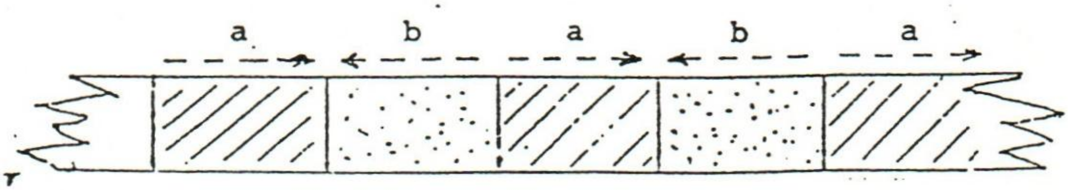

Fig. 1. PITS. Diagrammatic View of Section of Tape, Showing Alternating Blocks of Information

so that alternate blocks ("a" in Fig. 1) would be read or written in one direction with a space between successive blocks ("b" in Fig. 1) which would then be used as information when reading or writing in the other direction.

Only three engineering test models of this tape drive were built. In operation, the tape drive sounded like a machine gun, because the tape started and stopped at every block, 100 times per second; the bending and snapping of tape delivered an explosive cracking sound. Of course, a more-or-less sound-proof housing was built, which tended to muffle the noise. In June 1954, serious personnel losses on the part of the contractor, as well as delays and cost overruns, led to the termination of this work.

About two months after work on NOMAD ended Raytheon proposed to market commercially a computer to be called "RAYCOM" which differed only mildly from the NOMAD basic design. Later in 1954 a co-operative arrangement between Raytheon Corporation and Minneapolis-Honeywell led to formation of the Datamatic Corporation, and this resulted in launching the Datamatic 1000, first in a series of Honeywell computer models. Raytheon's share in the Computer Division of Honeywell was finally liquidated, and the H-series computers continue to flourish successfully.

Another commercial-market result from the NOMAD experience came about when, shortly before cancellation, several top Raytheon engineers on the project resigned to form a new company. The Computer Control Corporation (usually known as "3-C") began marketing a line of "building blocks" or circuit cards which were designed for flexible recombination into various configurations. These 3-C cards were partly based on developments under the NOMAD contract, and were moderately successful. Computers built from 3-C cards were among the earliest small computers in the country.

One other way in which NSA influenced the computer industry was through the wartime experience gained in cryptologic organizations by personnel who joined or returned to industry. IBM engineers in these organizations during World War II, after contributing to the advancement of information processing techniques, returned to IBM where they were very influential in the development of an experimental system of electronic tape processing machines. This TPM system led to the IBM 702, IBM's first computer designed especially for information processing.

IMPACT ON GENERAL DATA HANDLING

Because requirements for computer support are often dominated by the need for statistical and other analyses of great masses of data, the Agency quite early became preoccupied with improvements in input-output, conversion, and recording equipments. Quite often, also, the internal processing operations have been logical or transformational, rather than strictly computational. This preoccupation with "information processing" as contrasted with computing was responsible for several early (pre-computer) developments. For example, punched-card specialists in NSA's predecessor agencies in the 1930's developed procedures for indexing data for analysis, probably before anyone in industry. Long before the advent of modern computers, many variations of the procedure later known to computer users and programmers as "Key Word in Context" (KWIC) were in operation at ASA and CSAW with punched-card equipments. The section "Pre-Computer NSA" mentioned applications involving punched card and punched tape equipment, and special attachments to card and tape machines. One of the earliest commercial high-speed line printers came about because of NSA support, based at least partly on experimentation and initiatives by Agency engineers. Likewise, one of the first practical character-sensing machines received early encouragement from NSA in the form of a development contract. And much later, after commercial computers were becoming available, several developments by commercial firms became viable only after testing of first models by NSA engineers, with modifications and improvements made as a result of such tests.

TAPE STANDARDIZATION. We recall one situation where NSA action resulted in tangible savings for consumers of computer-grade magnetic tapes. In the mid-1950's, NSA use of magnetic tapes was just beginning to grow, and showed promise of soon involving great numbers of reels of tape. The available sources of supply were few, and information was lacking on which to base specifications of tape characteristics to be met by vendors. There was already some evidence that a very few large firms might dominate the industry. Not only might this have a monopolistic effect on prices, but the technical characteristics of the tape might be influenced. In the absence of strict enforceable specifications and standards, it was not possible to support attempts to encourage and develop alternate sources of supply.

The engineers in NSA's research group concerned with this situation recommended, in 1957, the establishment of a small laboratory equipped to test magnetic tapes from various sources. The purpose was to arrive at detailed specifications for "standard" computer tape which could be proved and duplicated. Tolerances for magnetic coating, backing characteristics, wear quality, and the like, were among the detailed requirements to be established. Also, environmental effects such as those due to temperature and humidity were to be studied, and techniques for cleaning and rehabilitating tape for re-use were also to be perfected. The laboratory and equipment built to perform tests leading to tape specification cost upwards of one million dollars. In 1962 the draft of tape spec's was circulated for manufacturers' comments, and in 1963, when spec's were published, the price of magnetic tape had already started to come down. In 1966 NSA established its "Qualified Products List" (QPL) and began negotiations to have the equipment and certification function taken over by another government agency. In 1967 NSA began transferring the testing function, including equipment and several trained technical people, to a joint GSA/NBS operation, where routine competitive procurement of computer tape for the entire federal establishment has been conducted ever since. Among the benefits accruing from these standardization and coordination efforts was the establishment at the National Bureau of Standards of a "standard" for magnetic tape. It is worth noting that by that time (1967) the price per reel had come down to about $12, from a maximum of $150. Even though the growing market for magnetic tape would have brought the price down somewhat, it is undoubtedly true that NSA's initiatives were responsible for hastening the process.

NSA'S SECOND GENERATION COMPUTERS:

SOLID STATE MACHINES

BOGART. The original impetus for BOGART (named after John B. Bogart, a famous city editor of the New York Sun) came from the early realization that data conversion, formatting, and the like often occupied a large proportion of the programmers' attention. Often special-purpose equipment had to be built to convert data from one medium to another. And the likelihood of needing all the power of the largest computers for sophisticated analyses suggested that it would pay to use a different "editing" computer to prepare data for input to such jobs. The original idea for BOGART's unit of manipulation was therefore the character (alphabetic or numeric), and the word size of 7 bits was specified in the December 1953 proposal. The logical design provided for three-word instructions, both core and drum memory, and input-output using both punched cards and punched paper tape. E.R.A. in July 1954 contracted to build two models, using diode and magnetic core logic for arithmetic and control. Cycle time of the core memory was 20 microseconds, and drum storage was eliminated.

In July 1955 the contract was modified to provide for construction of four instead of two machines, and to allow for connection of IBM Type 727 magnetic tape drives. These tape drives had become practically the standard for the industry. The logic design was also changed -- the word size became 24 bits, with capability of selecting any of three 8-bit portions of a word. Also, several index registers were provided. The four machines were delivered between July 1957 and January 1958. The pilot model of BOGART was subsequently modified, and in December 1959 became the fifth BOGART to come to NSA -- it was used as the central computer for ROB ROY, a remote-operated system with five outstations.

The BOGART computers were very reliable, and were used on a great variety of problems. Probably their original intended application -- editing and formatting -- became less emphasized because of BOGART's capabilities for higher-priority work and because other cheaper equipment became available for editing.

The influence of BOGART can probably be seen in both its engineering and logic sides. First, BOGART was probably the first U.S. computer which used "design automation" techniques. Also, many features of the logic design were unique and carried over into the family of Navy Tactical

Data System computers. Also the UNIVAC 490 includes features such as its index registers and "repetition" which were borrowed from or were influenced by BOGART. Control Data Corporation's CDC 1604 and CDC 160 also reflected early BOGART design experience of that company's founders.

SOLO. By January 1955, the use of transistors in place of electron tubes became increasingly likely, and their apparent advantages over tubes in smaller size, lower heat dissipation, and improved reliability set the stage for the coming of the new smaller mass-produced computers. At NSA the initial step in anticipation of these exciting changes was to begin training a small group of engineers in using the new components, and to form the nucleus of what became the transistor generation.

Among the projects under way at this time was a proposed remote-operation computer, which would place terminals in work areas. An alternative proposal to accomplish the same objective was to acquire a number of small computers, built with the new transistors as principal circuit component, and place each desk-size computer in a different area. A project "SOLO" was set up to build the first such machine and the decision was made to duplicate the logic design of ATLAS II. In June 1955, Philco Corporation was awarded a contract to build this machine, because Philco at the time was the only firm making reliable surface-barrier transistors (a short-lived technology which was superseded by junction transistors). Subcontracts for construction of SOLO's core memory and power supplies went to Remington-Rand-UNIVAC and Magnetic Controls Corporation, respectively.

During construction, there were many difficulties to be overcome, including troubles with subcontractor-furnished power supplies and memory. Also, after delivery in March 1958, NSA engineers spent about a year debugging the equipment. Although SOLO was logically a copy of ATLAS II, its memory lacked the supplemental drum of ATLAS II and its input output equipment was not very reliable, so that SOLO was not used on large operational problems. Because of these difficulties and delays, the original plan to build many copies of SOLO was abandoned, and the one desk-model SOLO was used for several years for testing other equipment and for training.

The original objectives -- (1) to prove that a reliable computer could be constructed using direct-coupled transistor logic, and (2) to train NSA engineers in transistor technology -- were attained. SOLO also holds the distinction of being the first completely transistorized computer in the United States. Philco built a commercial version, marketed with the designation TRANSAC S-1000. A larger improved computer, the TRANSAC S-2000, based on the Navy CXPQ computer, later called Philco S-2000, was marketed with more success.

HARVEST. Undoubtedly the most sophisticated computer of the second generation, NSA's HARVEST was one of the limited number of systems built by IBM as an embodiment of a research program called "STRETCH." Beginning in 1954 the planners at IBM had decided that, based on experience in operation of their first successful models (IBM 701 and 704, 702 and 705), a quantum leap ahead would be possible, if they could achieve an increase in circuit speed, lowered memory access time, improved logical design, and higher speed and capacity tapes and disks. A project was launched within the company's research laboratories whose goal would be to "stretch" the state of engineering art in the following general areas:

(1) Circuitry. If the 704 generation could be characterized as using one-megacycle circuitry, the new components (faster transistors, miniaturized circuits) could be expected to achieve the equivalent of ten-megacycles-per-second pulse rate.

(2) Memory. To keep a reasonable balance among the computer's component parts, the memory speed had to be increased (i.e. access time decreased) in proportion as circuit speed went up. At this time a goal of 2 microseconds access time for large memories (16,384 words) and 0.5 microsecond for small memories (1,024 words) was considered attainable.

(3) Magnetic Tapes, Disks. To supplement internal memory, it was originally proposed to develop a one-million-word capacity disk memory with transfer rate approximately 250,000 words per second. Later, it was found that certain applications would be better served by large-scale tape storage for external memory.

(4) Logic Improvements. In order to achieve an over-all performance of 100 times that of the 704, several types of logical design improvements showed promise. Here the guiding principle was the minimization or elimination of what most programmers refer to as "housekeeping" tasks. Thus, address modification could be made nearly automatic by any of several types of indexing schemes; a novel feature which became known as "look-ahead" provided for anticipating adjustments; use of tables could be a time-saver for switching indicators, specialized conversions, or even as a substitute for otherwise complex logical operations.

IBM experiments along these lines had progressed, by the spring of 1955, to the point where it was considered desirable to test the new ideas by constructing a "STRETCH" computer.

IBM decided to approach the two government agencies most likely to have both requirements for large-scale computer support and high probability of obtaining sufficient funding: NSA and Atomic Energy Commission.

The IBM STRETCH proposal came to NSA (May 1955) at a propitious time. The requirement for a large-volume data processor and the effort to satisfy that requirement under the ill-fated NOMAD project had been followed by a proposal, called FARMER, made in the spring of 1954, for a modular system of general-purpose and special-purpose machines. By providing flexibility in choosing such modules, it was the intention to maximize the advantages of both special-purpose and general-purpose equipments while minimizing their respective disadvantages. Thus, input-output, data editing, computation, and general storage requirements could be accommodated by a powerful and versatile computer, while problem needs which justified additional power could be met by special attachments, designed to operate with the main FARMER computer. A FARMER-NOMAD Special Study Group had been created; its members spent several months interviewing specialists in various Agency problem areas. Their report recommended that the FARMER approach be followed in future large-scale systems planning, and made several specific technical comments. Thus the reaction of Agency computer specialists to the logic ideas in IBM's STRETCH was immediate: this kind of system could become the first embodiment of FARMER.

Although IBM's offer to build a STRETCH computer for the Agency for $3,500,000 was considered to be a bargain, it was rejected for the following reasons:

(1) Two important components of the proposed system -- fast (0.5 microsecond access) memory and advanced magnetic tape external storage --were considered not well-enough developed.

(2) Over-all system logic was not sufficiently directed towards NSA requirements to qualify as the basis for FARMER.

After some negotiations, an agreement was worked out which provided for additional research by IBM in the areas of high-speed memory and high-density tapes and tape transports, and for logical design studies, partly supported by NSA funding.

The IBM proposal to Atomic Energy Commission in 1955 was accepted, after several months' delay, and a contract for delivering a STRETCH computer to AEC was signed in 1956. AEC's computer requirement emphasized high speed multiplication, whereas NSA's emphasis was on manipulation of large volumes of data and great flexibility and variety in non-numerical logical processes. Thus, in approximately the same time-frame, IBM was engaged in planning two embodiments of the STRETCH computer for two clients having widely differing requirements. In addition, IBM wanted to be ready for a possible commercial market.

IBM's computer architects settled on the following general outlines of a STRETCH system which purported to satisfy all three customer situations:

(1) A Central Processing Unit (CPU) which included logical and arithmetic capabilities;

(2) A variable number of 16,384-word memory banks, 2.18 microsecond access time;

(3) A floating point attachment whose operation was intimately involved with the CPU (note overlap indicated in Fig. 2);

(4) A bus system and input-output exchange, permitting communication among CPU, memory modules, and proposed future attachments.

By May 1957 a design proposal for NSA's model of STRETCH was ready. A rather careful evaluation effort was soon under way. The ad hoc group created to examine the design proposal made time estimates for executing candidate jobs and proposed several design improvements. The result of the group's studies was a favorable recommendation -- the proposed system was estimated to be faster than current equipment, in most cases by factors between 100 and 200. After more negotiations, final contract ratification was completed on 30 April 1958.

The STRETCH model (HARVEST) which was delivered to NSA in February 1962 was basically the same as other STRETCH systems. Besides the four units listed above, it had the following additional units (See Fig. 2):

(5) Two banks, 1,024 words each, of high-speed memory (0.9 microsecond access time);

(6) HARVEST Attachment, containing Streaming Unit and associated features for performing special statistical and other complex logical operations (note overlap with CPU, Fig. 2);

(7) High-Speed Exchange and high-speed, large-volume magnetic tape external storage unit (TRACTOR), with automatic features for loading and accessing tape cartridges.

TRACTOR was notable principally because of its (1) automatic features, (2) speed, and (3) total storage capacity. There were three automatic cartridge handling units, each capable of automatically seeking and extracting a specified cartridge under program control. Mounting, positioning, and threading of tape cartridges were entirely automatic. The total number of cartridges was 160, permitting an estimated total volume of data stored equal to 88 billion characters. Packing density on 1.75-inch-wide tape was 3000 bits per inch, and tape moved at 235 inches per second, yielding instantaneous information-transfer rate of 1,128,000 characters per second. Automatic checking and error-correction was provided, based upon inclusion of 6 check bits along with 16 information bits.

Additional massive programmer training and software development efforts were required in order to utilize HARVEST's powerful new features. Because of its logical complexity, the system's great potential came into its own only gradually. HARVEST was used for 14 years with emphasis on jobs not even conceivable for any other computer. It functioned very well throughout, and to the surprise of many, even the TRACTOR tape transports turned out to be quite reliable.

As already noted, HARVEST was a unique embodiment of the STRETCH computer development; that is, no successor was built, and no commercial models were ever contemplated. HARVEST's most important effect was undoubtedly on the engineers who designed it, since it was a program which brought out the best in all who were involved. HARVEST also exerted a great influence on specific computer developments, in several ways:

(1) Logic technology used in IBM's 7000-series and subsequent models followed the STRETCH and HARVEST foundation.

(2) HARVEST and STRETCH 2-microsecond core memories were used in IBM's 7090 and other computers.

(3) The TRACTOR Tape System was the first completely automated tape library. This system also pioneered the use of error-correcting codes and de-skewing buffers.

(4) HARVEST data-flow was unique, but the pipeline-design experience enabled IBM engineers to successfully design other machines, such as the Model 91.

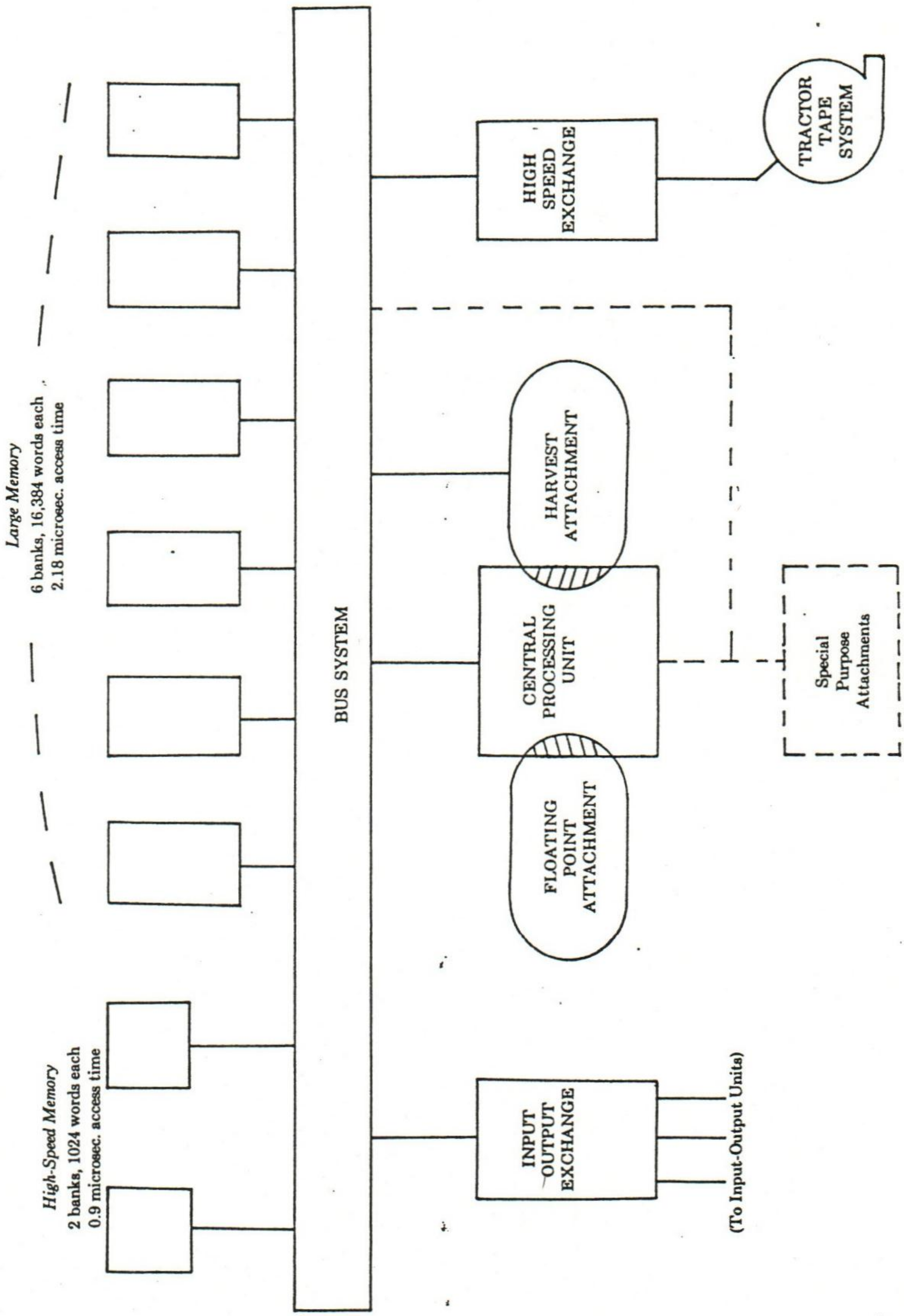

Figure 2 .—HARVEST System Block Diagram

TOWARD THE COMPUTER OF THE FUTURE:

LIGHTNING

One of the most costly as well as far-reaching research programs ever undertaken by NSA was born at a cocktail party in July 1956. The story is told of a conversation involving several high-level NSA equipment planners and Lt. Gen. Ralph J. Canine, then Director, NSA (died 1969). There had been some discussion of NSA's perennial problem: the race between analysts' insatiable requirements for new ways to attack always-increasing volumes of data and engineers' efforts to design and build bigger and faster computers to meet these needs. Apparently no matter how powerful the new equipment, we never seemed to catch up. The then-current development, HARVEST, was being designed to fill such requirements with an estimated 100-fold improvement over the best current computers, and its completion was several years away. Gen. Canine then forcibly expressed his exasperation by exploding, "Damit, I want you fellows to get the jump on those guys! Build me a thousand megacycle machine! I'll get the money!" Within the next few days, the LIGHTNING project was under way, with a budget of 25 million dollars for a five-year effort to develop "thousand megacycle" electronics.

The LIGHTNING project received approval of the Deputy Defense Secretary in October 1956, and was endorsed at the Presidential level in a White House conference in December 1956, by Dr. James Killian, with President Eisenhower's backing. Actual work by several contractors was under way in June 1957, the start of a projected five-year program with a funding level of approximately $5 million per year.

In preparation for starting work on LIGHTNING, the following guiding principles were laid down:

(1) Several lines of research would be pursued in parallel. "Non-conventional" devices and circuits would be backed, based on information indicating adequate other support of "conventional" techniques.

(2) Practicability of components developed under the program would be verified by construction of test equipments at appropriate stages.

(3) Results of the research would be reported in open literature and made freely available. Sponsored symposia and special sessions at

standard symposia would be another medium for exchange of technical information.

Much of the discussion in the earliest stages of LIGHTNING revolved around clarification of the oft-repeated expression "kilomegacycle computer." Rather than a computer operating at a thousand million pulses per second, the objective was an analytic system accomplishing tests a thousand times as fast as current megacycle equipment. This thousand-fold power increase could be expected to be achieved by (a) faster circuitry, (b) better logic, and (c) other over-all system improvements. LIGHTNING researches were primarily directed towards the first of these -- faster circuitry -- with every effort aimed at the ultimate goal of a performance improvement by a factor of one thousand.

The following is a brief summary of the main lines of research supported by LIGHTNING, and the contractor on each:

(1) Sperry Rand UNIVAC (SRU); Research on magnetic film devices and circuits. To prove the high-speed capabilities and feasibility of thin film magnetic memories and certain functional array logic assemblies, a LIGHTNING "Test Machine" was planned, constructed and tested in 1962. Its memory access time was 150 nanoseconds (ns-billionths of a second). SRU also tested logic circuits using tunnel diodes, in a serial arithmetic logic tester. These circuits were operated at 4 ns per logic level.

(2) Radio Corporation of America (RCA): Tunnel diodes. RCA built all-tunnel-diode logic and memory subsystems and interconnected the two subsystems in 1962. The logic circuits operated with delays down to 1 ns delay time and repetition rates of approximately 200 mc/sec. Still faster counting and shifting circuits were demonstrated in a 40-gate subsystem.

(3) International Business Machines Corporation (IBM): Cryogenics; superconducting films. Ever since the late Dudley Buck's report of his invention of the cryotron (1958), many laboratories have pursued attempts to build practical high-speed computing elements, using as a switching basis the superconducting property of certain materials at low (near absolute zero) temperatures. IBM's 1960 report for Phase II mentions their construction of a superconducting flip-flop which switches in 2 ns. Their work on machine organization included memory circuits which also performed various logic functions. NSA support for this research was discontinued in 1961 because too much time would be required for development of fast and reliable components. However, the work was followed by other investigations and is still alive today. (See below)

(4) Philco Corporation: High-speed rotary switch. The logical design for a 48-position rotary switch and permuter was completed; the stepping rate was 40 megapulses per second, including transmission of 6 serial bits through the device. A feasibility model was built, using several hundred transistors, which stepped at 40 million times per second.

(5) General Electric Company (GE): Pumped tunnel diode-transistor logic. The feasibility of circuits based on the pumped tunnel diode was demonstrated by the successful operation of a 100-mc pseudorandom sequence generating circuit using 80 modules. In 1961 this work was picked up on other GE (Syracuse) contract programs outside LIGHTNING.

(6) Massachusetts Institute of Technology Research Laboratory for Electronics (MIT): Investigation of computer organization, basic electronic materials properties, and revolutionary computer device construction techniques. Voluminous output of publications and theses by graduate students and others.

(7) University of Kansas: Nanosecond pulse techniques, pulse generation, transmission, detection, characterization, display, and parameter measurement. Assistance in research on high-speed instrumentation.

(8) Ohio State University: Investigation of klystron bunching as a means to generate fast rise time, high repetition rate, and large amplitude (all simultaneously) pulses in low impedance circuits. A special electron tube was designed, tested, and two were delivered which did satisfy these requirements. But now this type of vacuum tube equipment has been superseded by solid state devices.

Progress reports by contractors on work referred to above were supplied directly to AEC, several Air Force laboratories, ONR, and other government organizations. In addition, the BuShips presented, on three different occasions, three-day symposia featuring reports by the contractors, for interested government organizations and laboratories. Published articles in recognized technical journals numbered over 160, and many papers were presented at major technical conferences. A total of 320 patent applications and 71 university theses were written as a result of LIGHTNING.

Among direct payoffs from LIGHTNING, there was requirement in the address-selection matrix in the high-speed memories of HARVEST for a faster diode. Sperry Rand's Norwalk plant developed, under LIGHTNING sponsorship, a silicon high-conductance avalanche diode which satisfied the requirement. Many other techniques and components which came out of LIGHTNING research were used in special-purpose machines for NSA and for other defense agencies. For example, Sperry Rand developed, under LIGHTNING sponsorship, one of the earliest techniques for strip-line manufacture. And what may have been the first magnetic thin film content-addressed memory was built by the same firm. Many areas of electronic data processing began to make use of LIGHTNING nanosecond techniques. For example, the UNIVAC Model 1107, first delivered in 1962, made use of thin film techniques for fast memory. Also, LIGHTNING undoubtedly was responsible for inducing commercial firms to speed up their own advanced research efforts. However, most computers which began to come on the commercial market following the time of LIGHTNING researches relied principally on developments in semi-conductors and microminiaturization which could more readily be reproduced in quantity, such as transistors and integrated circuits.

Although LIGHTNING support for IBM research in cryogenics was discontinued in 1961, as mentioned earlier, the team of researchers at IBM continued work in this field, although at a somewhat curtailed strength. Several years later, the discovery of ways of putting to practical use the phenomenon known as the Josephson Junction led to a new surge of interest in cryogenics. NSA again contributed partial financial support to speed these developments. It now appears that these high-speed (several picoseconds (=one-trillionth sec.) - range gating time), low power-dissipation components show promise as a possible candidate for the future computer generation.

COMPUTER RESEARCHES AFTER LIGHTNING. It is generally agreed that the computer industry in the 1970's is approaching maturity. That is, the established leaders in the field are sufficiently secure that budgets for research can be supported for the most part without U.S. assistance.

CONCLUSION. In simple terms the NSA mission has always been to develop and to protect information. The technical processes required to perform this mission, although quite intricate at times, were carried out entirely without machine assistance in the early 1930's. As the complexity of the technical processes increased, Agency specialists sought the help of machines. World War II gave increased impetus to the use of machines as NSA's predecessors enlisted the help of U.S. private industry in developing the machinery needed.

Although the modern electronic computer did not come along in time to assist in the war effort, several pre-computer special-purpose equipments built for NSA under contract, as we have seen, utilized electronic digital techniques. To the extent that the contractors involved gained early experience with digital circuits, NSA certainly hastened the start of the computer age. And experience gained in the development of large-scale systems for NSA, up to and including HARVEST, resulted in design improvements for commercial computers. Finally, the great impetus from LIGHTNING inspired many discoveries at the level of fundamental materials properties, high-speed circuitry, and components fabrication -- discoveries which assisted in the birth of another computer generation.

APPENDIX A

Chronology of NSA Computer "Firsts"

Date	Event Description
Oct 1948	DEMON placed in operation. First practical use of magnetic drum for data storage for analytic operations at electronic speeds.
Dec 1950	ATLAS I delivered; operational in one week. First parallel electronic computer in U.S. with drum memory. Forerunner of commercial E.R.A. 1101.
Apr 1952	ABNER operational; designed and built at NSA. Serial computer similar in logic to SEAC and EDVAC. Most sophisticated computer of its time. First use of computation simultaneous with input-output. Most complete complement of input-output capabilities (punched cards, punched paper tape, magnetic tape, parallel printer, typewriter, console).
Oct 1953	ATLAS II delivered; forerunner of commercial E.R.A. 1103 (UNIVAC Scientific 1103). Model 2, delivered in November 1954, equipped with core memory instead of electrostatic store; first core memory computer delivered to customer in U.S.
July 1957	First BOGART delivered. Believed to be first practical computer using magnetic (diode/core) logic in basic circuitry. Believed to be first computer to utilize design automation. Influenced design of several commercial models built by UNIVAC and Control Data Corp.
Mar 1958	SOLO delivered; first completely transistorized computer in U.S. Model for Philco's TRANSAC S-1000 and forerunner of improved S-2000.
June 1957	LIGHTNING high-speed circuitry researches under way. Believed to be largest U.S. government computer research support. Influenced many commercial developments.
Feb 1962	HARVEST delivered; most sophisticated model of STRETCH series. The TRACTOR tape system was the first completely automated tape library. Influenced design of IBM System 360.

APPENDIX B

THEORY AND TECHNIQUES

FOR DESIGN OF ELECTRONIC COMPUTERS

Lectures given at the Moore School

8 July 1946 - 31 August 1946

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NOTE: The complete texts of most of the lectures, whose titles appear on the following pages, are contained in the following reports issued by the Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, Pennsylvania:

Report Number	Volume	Date	Lectures
47-21	I	10 Sep 47	1 - 10
47-24	II	1 Nov 47	11 - 21
48- 9	III	30 Jun 48	22 - 33
48-10	IV	30 Jun 48	34 - 48

APPENDIX B (continued)

1. Introduction to the Course on Electronic Digital Computers
   George Stibitz

2. The History of Computing Devices
   Irven Travis

3. Digital and Analogy Computing Machines
   John W. Mauchly

4. Computing Machines for Pure Mathematics
   D. H. Lehmer

5. Some General Considerations in the Solution of Problems in Applied Mathematics
   D. R. Hartree

6. Numerical Mathematical Methods-I (Summary only)
   Herman H. Goldstine

7. Numerical Mathematical Methods-II (Summary only)
   Herman H. Goldstine

8. Digital Machine Functions
   Arthur H. Burks

9. The Use of Function Tables with Computing Machines
   John W. Mauchly

10. A Preview of a Digital Computing Machine
    J. P. Eckert Jr.

11. Elements of a Complete Computing System (Summary only)
    C. B. Sheppard

12. Numerical Mathematical Methods-III (Summary only)
    Herman H. Goldstine

13. The Automatic Sequence Controlled Calculator
    Howard H. Aiken

14. Electro-Mechanical Tables of the Elementary Functions
    Howard H. Aiken

APPENDIX B (continued)

15. Types of Circuits-General
    J. Presper Eckert, Jr.

16. Switching and Coupling Circuits
    T. K. Sharpless

17. Numerical Mathematical Methods-IV
    Arthur W. Burks

18. Numerical Mathematical Methods-V (Summary only)
    Herman H. Goldstine

19. On the Accumulation of Errors in Numerical Integration on the ENIAC
    Hans Rademacher

20. Reliability of Parts
    J. Presper Eckert, Jr.

21. Memory Devices
    C. Bradford Sheppard

22. Sorting and Collating
    John W. Mauchly

23. Adders (Abstract only)
    J. Presper Eckert, Jr. and C. B. Sheppard

24. Multipliers (Abstract only)
    J. Presper Eckert, Jr.

25. Conversion Between Binary and Decimal Number Systems
    John W. Mauchly

26. Numerical Mathematical Methods-VI (Title only)
    Herman H. Goldstine

27. Magnetic Recording
    Chuan Chu

28. Tapetypers and Printing Mechanisms
    J. Presper Eckert, Jr.

29. A Review of Government Requirements and Activities in the Field of Automatic Digital Computing Machinery
    J. H. Curtiss

APPENDIX B (continued)

30. Numerical Mathematical Methods-VII (Title only)
    Herman H. Goldstine

31. Numerical Mathematical Methods-VIII
    Arthur H. Burks

32. Applications of Digital Computation Involving Continuous Input and Output Variables (Title only)
    Perry Crawford, Jr.

33. Continuous Variable Input and Output Devices
    J. Presper Eckert, Jr.

34. Reliability and Checking in Digital Computing Systems
    S. B. Williams

35. Reliability and Checking
    J. Presper Eckert, Jr.

36. Code and Control-I (Title only)
    C. B. Sheppard

37. Code and Control-II: Machine Design and Instruction Codes
    J. W. Mauchly

38. Code and Control-III (Title only)
    C. B. Sheppard

39. Code and Control-IV: Examples of a Three-Address Code and the Use of 'Stop Order Tags'
    Calvin N. Mooers

40. New Problems and Approaches (Title only)
    John von Neumann

41. Electrical Delay Lines (Title only)
    J. Presper Eckert, Jr.

42. A Parallel-Type EDVAC (Title only)
    J. Presper Eckert, Jr.

43. The Selectron
    Jan Rajchman

44. Discussion of Ideas for the Naval Ordnance Laboratory Computing Machine
    Calvin N. Mooers

APPENDIX B (Concluded)

45. A Parallel Channel Computing Machine
    J. Presper Eckert, Jr.

46. A Four-Channel Coded-Decimal Electrostatic Machine (Summary only)
    C. B. Sheppard

47. Description of Serial Acoustic Binary EDVAC
    T. K. Sharpless

48. Accumulation of Errors in Numerical Methods (Title only)
    J. W. Mauchly

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